* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention is applied to the failure analysis in the development stage of the new process of the semiconductor integrated circuit equipment large-area[high integration and]-ized especially about the semiconductor integrated circuit equipment which carried TEG (Test Element Group), and relates to an effective technique.
[0002]
[Description of the Prior Art] Conventionally, the process development of new semiconductor integrated circuit equipment and the process evaluation using the test pattern as one of the technique effective in management data collection of a mass production line occur. The process evaluation using said test pattern performs various electric measurement by TEG (Test Element Group) completed at all the processes or the partial process of production of said semiconductor integrated circuit equipment, and acts as the monitor of the property of actual equipment. What is used for acquisition of the so-called process parameter of values, such as a processing dimension obtained by the basic process among said TEG, the depth, and precision, etc. is called Process TEG.
[0003] The semiconductor integrated circuit equipment which carried said TEG is divided into some classes by the utilization object of the TEG. In the phase of said process development, the TEG wafer with which said process TEG was formed in all the fields that mainly serve as the whole semi-conductor wafer surface or a chip is used. Moreover, what formed Process TEG by considering a part for two or more places of the field used as the chip of the wafer for production of the semiconductor integrated circuit equipment (device) used as a product or a single tier as the chip for TEG, and the thing which formed Process TEG in some chips used as a device are used for said management data collection.
[0004] Moreover, the process evaluation by logic diagnosis occurs besides the process evaluation using said test pattern. By the process evaluation by said logic diagnosis, various kinds of flow inspection is conducted using said device, and the inspection result is compared with the result (expected value) of original obtained on a circuit design. When said inspection result and expected value differ from each other, it assumes that somewhere in components formed into the device or wiring have a defect, logical operation is performed, and the class of a reason fault and defect is specified.
[0005] In said TEG or the process evaluation by logic diagnosis, the defect generated in the manufacture process of a device is detected and analyzed efficiently, and it is important for a process feedback or to act as feedforward and to raise the quality of a process.
[0006]
[Problem(s) to be Solved by the Invention] However, in said Prior art, indication and failure analysis of a defect location are becoming difficult with high integration and large-area-izing of the semiconductor integrated circuit equipment (device) used as a product. Especially, by installation of the multilayer-interconnection technique accompanying high integration of a device, since the number of metal wiring which connects the semiconductor device formed on the semi-conductor substrate becomes huge, detection of a poor open circuit (opening) of said metal wiring and a poor short circuit (short circuit) and

analysis are becoming difficult.
[0007] In the process evaluation using said test pattern, a test pattern must be formed for every item to evaluate. for example, in order to evaluate poor opening and short [poor] of a case, [of four layer wiring by installation of a multilayer-interconnection technique] The test pattern for evaluating poor opening of metal wiring of each wiring layer Four The test pattern of five, 13 [i.e.,], is needed for the test pattern for evaluating the flow of a through hole whose test pattern for evaluating short [poor] connects connection of the semiconductor device formed on four and a semi-conductor substrate and metal wiring, and metal wiring of each wiring layer.
[0008] Since the area which forms the test pattern of each item assigned in one chip will become small and the number of each test patterns will decrease if an item to evaluate increases, possibility that a defect will not be detected from said test pattern becomes high. Moreover, if there are few test patterns, the number of failures of as opposed to the total of a test pattern also in defects increasing in number for a while (failure consistency) will become large.
[0009] In the process evaluation using said test pattern, since failure with a test pattern was investigated and it considers that the failure consistency of the test pattern is the failure consistency of a actual device instead of investigating failure of a actual device, the test pattern must be reflecting the circuit pattern in a actual device enough. However, since the item evaluated by installation of the part, the multilayer-interconnection technique, etc. which the degree of integration of a actual device became high is increasing, the degree of integration of a actual device cannot make high the degree of integration of said test pattern. Therefore, there was a problem that it was difficult to consider that the failure consistency obtained from a test pattern is a failure consistency in a actual device, and to feed it back to a process.
[0010] Moreover, when it was assumed that the process evaluation by said logic diagnosis has two or more defects in one chip, logical operation became complicated, since it was very difficult to point out the class of the defect location and defect and time amount was taken, like the initial stage of process development, when there was much failure, defect detection was difficult, and there was a problem that the effectiveness of failure analysis was bad.
[0011] The object of this invention is to offer the technique which can make easy high integration and defect detection of the large-area-ized semiconductor integrated circuit equipment. Other objects of this invention are to offer the technique which can be improved in the effectiveness of the failure analysis of the large-area[high integration and]-ized semiconductor integrated circuit equipment. Other objects of this invention are to offer the technique which can integrate highly the test pattern which evaluates the process of semiconductor integrated circuit equipment. Other objects of this invention are in the defect detection approach of semiconductor integrated circuit equipment to offer the technique which can point out the location of two or more defects who exist in one semiconductor integrated circuit. As new along [said] this invention a description as the other objects will become clear by description and the accompanying drawing of this description.
[0012]
[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.
[0013] (1) Said defect detection gate circuit which has the test pattern which can detect a poor open circuit and poor short circuit of metal wiring which connects two or more semiconductor devices which are semiconductor integrated circuit equipment which has a defect detection gate circuit, and were formed on the semi-conductor substrate The defect detecting element connected in the direction of X train, and the direction of Y train in the shape of a matrix, [many] X train selector and Y train selector which choose one defect detection gate circuit which serves as an object for defect detection with the select signal set up beforehand out of said many defect detection gate circuits, The decoder circuit which generates said poor open circuit and the data signal for poor short circuit detection, The data signal line which inputs the data signal for said defect detection into said each defect detection gate circuit and said X train selector, The detection data output line which outputs the defect detection result of each defect detection gate circuit where the data signal for said defect detection was inputted to said Y train selector,

X train selection signal line which inputs into said X train selector X train select signal which chooses the data signal inputted into the defect detection gate circuit used as said object for defect detection from the data signals inputted into said X train selector, Out of the defect detection result of each defect detection gate circuit inputted into said Y train selector Y train selection signal line which inputs into said Y train selector Y train select signal which chooses the defect detection result outputted from the defect detection gate circuit used as said object for defect detection, It is semiconductor integrated circuit equipment possessing the data output line which outputs the data signal inputted into the defect detection gate circuit used as said object for defect detection chosen by said X train selector and Y train selector, and the outputted defect detection result.

[0014] (2) Said defect detection gate circuit which has the test pattern which can detect a poor open circuit and poor short circuit of metal wiring which connects two or more semiconductor devices which are semiconductor integrated circuit equipment which has a defect detection gate circuit, and were formed on the semi-conductor substrate With the select signal set up beforehand out of the defect detecting element connected in the direction of X train, and the direction of Y train in the shape of a matrix, and said many defect detection gate circuits [many] Two or more defect detection partitions which have X train selector and Y train selector which choose one defect detection gate circuit used as the object for defect detection, The decoder circuit which generates said poor open circuit and the data signal for poor short circuit detection, The data signal line which inputs said data signal into the defect detection gate circuit and X train selector of each of said defect detection partition, The detection data output line outputted to Y train selector in which the defect detection result of each defect detection gate circuit where said data signal was inputted was prepared in said each defect detection partition, Out of said data signal inputted into X train selector of each of said defect detection partition X train selection signal line inputted into each of X train selector in which X train select signal which chooses the data signal inputted into the defect detection gate circuit used as said object for defect detection was formed in said each defect detection partition, Out of the defect detection result of each defect detection gate circuit inputted into Y train selector of each of said defect detection partition Y train selection signal line inputted into each of Y train selector in which Y train select signal which chooses the defect detection result of the defect detection gate circuit used as said object for defect detection was formed in said each defect detection partition, The partition data output line which outputs the data signal inputted into the defect detection gate circuit used as the object for defect detection chosen by X train selector and Y train selector of each of said defect detection partition, and the outputted defect detection result, The partition selector which chooses the defect detection result of one defect detection partition with the partition select signal set up beforehand out of said data signal outputted from said each defect detection partition, and a defect detection result, It is semiconductor integrated circuit equipment possessing the data output line which outputs the defect detection result of the defect detection partition chosen by said partition selector.

[0015] In the above (1) or the semiconductor integrated circuit equipment of (2) (3) Said defect detection gate circuit It consists of a test pattern prepared between the outgoing end of the 1st logical circuit and the 2nd logical circuit, and said 1st logical circuit, and the input edge of said 2nd logical circuit. Said test pattern It consists of metal wiring for poor detection which connected metal wiring formed in two or more wiring layers prepared on a semi-conductor substrate through the through hole formed between said each wiring layer, and wiring for poor short circuit detection formed for said every wiring layer so that said metal wiring for poor detection might be adjoined.

[0016] (4) The defect detecting element by which many defect detection gate circuits were connected in the direction of X train, and the direction of Y train in the shape of a matrix, X train selector and Y train selector which choose one defect detection gate circuit which serves as an object for defect detection out of said many defect detection gate circuits with the select signal set up beforehand, It is the defect detection approach of semiconductor integrated circuit equipment of providing the decoder circuit which generates the data signal for defect detection. X train select signal and Y train select signal which choose the defect detection gate circuit used as said object for defect detection are inputted into said X train selector and Y train selector. By said decoder circuit Generate the data signal for poor short circuit

detection, and the data signal for this poor short circuit detection is inputted into each defect detection gate circuit and said X train selector of said defect detecting element. The defect detection result of each defect detection gate circuit based on the data signal for the inputted poor this short circuit detection is inputted into said Y train selector. After recording the data signal inputted into said selected defect detection gate circuit and the poor short circuit detection result which are outputted from said X train selector and Y train selector, by said decoder circuit Generate the data signal for poor open-circuit detection, and the data signal for poor open-circuit detection is inputted into the defect detection gate circuit which inputted the data signal for said poor short circuit detection. The data signal inputted into said selected defect detection gate circuit and the poor open-circuit detection result which are outputted from said X train selector and Y train selector are recorded. About the defect detection gate circuit which changed said X train select signal and was connected in the one direction of Y train Record a poor sequential short circuit detection result and a poor open-circuit result, and said Y train select signal is changed. After recording the poor short circuit detection result of all defect detection gate circuits and the poor open-circuit detection result which repeated poor sequential short circuit detection and poor open-circuit detection, and were connected in the shape of a matrix, It is the defect detection approach of the semiconductor integrated circuit equipment which carries out specification of pinpointing of the defect detection gate circuit where the defect was detected and a poor open circuit, or a poor short circuit based on said poor short circuit detection result and a poor open-circuit detection result.

[0017] (5) The defect detecting element by which many defect detection gate circuits were connected in the direction of X train, and the direction of Y train in the shape of a matrix, Two or more defect detection partitions possessing X train selector and Y train selector which choose one defect detection gate circuit which serves as an object for defect detection out of said many defect detection gate circuits with the select signal set up beforehand, It is the defect detection approach of semiconductor integrated circuit equipment of having the decoder circuit which generates the data signal for defect detection, and the partition selector which chooses one defect detection partition from said two or more defect detection partitions with the partition select signal set up beforehand. X train select signal and Y train select signal which choose the defect detection gate circuit used as said object for defect detection are inputted into said X train selector and Y train selector. By said decoder circuit Generate the data signal for poor short circuit detection, and the data signal for this poor short circuit detection is inputted into each defect detection gate circuit and said X train selector of said defect detecting element. The defect detection result of each defect detection gate circuit based on the data signal for the inputted poor this short circuit detection is inputted into said Y train selector. The data signal inputted into said selected defect detection gate circuit and the poor short circuit detection result which are outputted from said X train selector and Y train selector of each defect detection partition are inputted into a partition selector. With said partition select signal Choose one defect detection partition from said each defect detection partition, and the data signal of a defect detection partition and the poor short circuit detection result which were this chosen are outputted and recorded from said partition selector. Said partition selector signal is changed, a sequential output is carried out and the data signal of all defect detection partitions and a poor short circuit detection result are recorded. By said decoder circuit Generate the data signal for poor open-circuit detection, and the data signal for poor open-circuit detection is inputted into the defect detection gate circuit which inputted the data signal for said poor short circuit detection. Are inputted into said partition selector from X train selector and Y train selector of each of said defect detection partition. The data signal inputted into said selected defect detection gate circuit, and a poor open-circuit detection result Output one at a time in order, record, and said X train select signal is changed. About the defect detection gate circuit connected in the one direction of Y train, a poor sequential short circuit detection result and a poor open-circuit result are recorded. Change said Y train select signal and poor sequential short circuit detection and poor open-circuit detection are repeated. After recording the poor short circuit detection result of all defect detection gate circuits and the poor open-circuit detection result which were connected in the shape of [of all defect detection partitions] a matrix, It is the defect detection approach of the semiconductor integrated circuit equipment which carries out specification of pinpointing of the defect detection gate circuit where the defect was detected and a poor open circuit, or

a poor short circuit based on said poor short circuit detection result and a poor open-circuit detection result.
[0018] Hereafter, this invention is explained to a detail with the gestalt (example) of operation with reference to a drawing. In addition, in the complete diagram for explaining an example, what has the same function attaches the same sign, and explanation of the repeat is omitted.
[0019]
[Embodiment of the Invention] (Example) Drawing 1 is the mimetic diagram showing the outline configuration of the semiconductor integrated circuit equipment which carried the process TEG of the example by this invention. drawing 1 -- setting -- CH -- for a defect detection partition and FBA, a defect detection partition field and D are [a semiconductor chip and B / the partition on a semiconductor chip CH, and FB / a partition selector and RT of a decoder circuit and BS] the RAM assessment TEG.
[0020] The semiconductor integrated circuit equipment which carried the process TEG of this example As shown in drawing 1 , have been arranged in two or more partitions on the semiconductor chip CH divided into the partition B of 196 beside [16] vertical 16x. The circuit which detects poor opening (open circuit) and short [poor] (short circuit) of metal wiring The poor opening short detection partition in which (a defect detection gate circuit is called hereafter) was prepared FB, decoder circuit D which generates the data signal for defect detection inputted into said defect detection partition FB, (A defect detection partition is called hereafter) It is constituted by the poor opening short detection TEG and the RAM assessment TEG (RT) which consist of a partition selector BS which chooses the defect detection result of one defect detection partition from the defect detection results outputted from said two or more defect detection partitions FB. Hereafter, the poor opening short detection TEG which consists of said defect detection partition FB, decoder circuit D, and a partition selector BS is called a gate matrix TEG. In the gate matrix TEG of this example, as shown in drawing 1 , said defect detection partition FB of 90 is formed by making the 90th division fraction on said semiconductor chip CH into the defect detection partition field FBA. Moreover, said decoder circuit D was prepared in the 16th division fraction near said defect detection partition field FBA, and the partition selector BS is formed in the 1st division fraction. In addition, in drawing 1 , wiring which connects between the defect detection partition FB of said gate matrix TEG, input decoder circuit D, and the partition selector BS is omitted.
[0021] Said RAM assessment TEG (RT) is TEG for evaluating actuation of RAM (Random Access Memory), and detection of metal wiring by the gate matrix TEG of this example opening short [poor] is unrelated. Therefore, it does not need to be prepared on said semiconductor chip CH. Moreover, other TEG may be formed instead of said RAM assessment TEG (RT). Moreover, partitions other than said defect detection partition field FBA on said semiconductor chip CH and the RAM assessment TEG (RT) are partitions which are not formed at all in order to investigate the calorific value of a semiconductor device.
[0022] Drawing 2 is the block diagram showing the outline configuration of the gate matrix TEG of this example. In drawing 2 FA1, XS1, YS1, OY1, XOX1, and XOY1, respectively The defect detecting element of the 1st defect detection partition FB1, X train selector, Y train selector, a detection data output line, a 1st partition X string data output line, a 1st partition Y string data output line, FA2 and XS2, respectively The defect detecting element of the 2nd defect detection partition FB2, X train selector, FA6 and XS6, respectively The defect detecting element of the 6th defect detection partition FB6, X train selector, FA87 and XS87, respectively The defect detecting element of the 87th defect detection partition FB87, X train selector, FA88 and XS88, respectively The defect detecting element of the 88th defect detection partition FB88, X train selector, FA90, XS90, YS90, XOX90, and XOY90, respectively The defect detecting element of the 90th defect detection partition FB90, X train selector, Y train selector, a 90th partition X string data output line, a 90th partition Y train output-data line, A decoding signal line, and D1 and D16 DS, respectively The 1st decoder circuit, the 16th decoder circuit, For X train selection signal line and XSOY, Y train selection signal line and BSK are [IX1 and IX16 / the 1st data signal line, the 16th data signal line, and XSOX / X string data output line and XOY of a partition selection signal line and XOX] Y string data output lines, respectively.
[0023] Although omitted in drawing 2 , in this example, the serial numbers from 1 to 90 are attached,

each of said defect detection partition FB of 90 is distinguished, and each will be called the n-th defect detection partition FBn (n is the integers from 1 to 90). Moreover, said decoder circuit of 16 also attaches and distinguishes the serial number to the 16th decoder circuit from the 1st decoder circuit.
[0024] As shown in drawing 2 , said 1st defect detection partition FB1 is constituted by the defect detection partition FA 1, X train selector XS1, and Y train selector YS1, and the 90th defect detection partition FB90 is similarly constituted from a gate matrix TEG of this example by the defect detecting element FA 90, X train selector XS90, and Y train selector YS90. Although the part is omitted in drawing 2 , said remaining n-th defect detection partition FBn (n is the integers from 2 to 89) is also constituted by the defect detecting element FAn, X train selector XSn, and Y train selector YSn, respectively.
[0025] The defect detecting element FA 1 prepared in said 1st defect detection partition FB1 and X train selector XS1 are connected with the 1st decoder circuit D1 by the 1st data signal line IX 1. Moreover, said 1st data signal line IX 1 is connected even with the defect detecting element FA 2 prepared in the 2nd defect detection partition FB2, and X train selector XS2 to the defect detecting element FA 6 prepared in the 6th defect detection partition FB6 and X train selector XS6 as shown in drawing 2 . The defect detecting element FA 90 which similarly was prepared in said 90th defect detection partition FB90 from the defect detecting element FA 87 prepared in the 87th defect detection partition FB87 and X train selector XS87, and X train selector XS90 are connected with the 16th decoder circuit D16 by the 16th data signal line IX 16.
[0026] Although the part is omitted in drawing 2 , the defect detecting element FAn and X train selector XSn which were prepared in said n-th defect detection partition FBn (n is the integers from 1 to 90) are connected with either from the 1st decoder circuit D1 to the 16th decoder circuit D16 by either from the 1st data signal line IX 1 to the 16th data signal line IX 16.
[0027] The decoding signal line DS is connected, and each from said 1st decoder circuit D1 to the 16th decoder circuit D16 changes into poor opening in the defect detecting element FAn of each of said n-th defect detection partition FBn, or the data signal for poor short detection the decoding signal inputted by said decoding signal line DS, and outputs it by the 16th data signal line IX 16 from said 1st data signal line IX 1. A data signal with said 1st data signal line IX 1 to the same 16th data signal line IX 16 is outputted.
[0028] It connects by the detection data output line OY, and the defect detecting element FA 1 and Y train selector YS1 which were prepared in said 1st defect detection partition FB1 output the defect detection result based on the data signal for defect detection inputted by said 1st data signal line IX 1 to said Y train selector YS1 by said detection data output line OY. At this time, two or more detection results are outputted from the defect detecting element FA 1 prepared in said 1st defect detection partition FB1. Similarly, although the part is omitted in drawing 2 The defect detecting element FAn and Y train selector YSn which were prepared in each n-th defect detection partition FBn (n is the integers from 1 to 90) It connects by the detection data output line OY, and the defect detection result based on the data signal for defect detection inputted from either of said 1st data signal line IX 1 to the 16th data signal lines IX 16 is outputted to said Y train selector YSn with said detection result output line OY. At this time, two or more defect detection results are outputted from the defect detecting element FAn prepared in said n-th defect detection partition FBn.
[0029] X train selection signal line XSOX and the 1st partition X string data output line XOX1 other than the 1st data signal line IX 1 which were connected with said 1st decoder circuit D1 are connected to X train selector XS1 prepared in said 1st defect detection partition FB1. Similarly, said X train selection signal line XSOX and the 90th partition X string data output line XOX90 other than the 16th data signal line IX 16 which were connected with said 16th decoder circuit D16 are connected to X train selector XS90 prepared in said 90th defect detection partition FB90.
[0030] Although omitted in drawing 2 , X train selection signal line XSOX and the n-th partition X string data output line XOXn other than either from said 1st data signal line IX 1 to the 16th data signal line IX 16 are connected to X train selector XSn prepared in said remaining n-th defect detection partition FBn (n is the integers from 2 to 89). The same X train select signal is inputted into X train

selector XS prepared in each of said defect detection partition FB of 90.
[0031] Y train selection signal line XSOY and the 1st partition Y string data output line XOY1 other than said detection data output line OY are connected to Y train selector YS1 prepared in said 1st defect detection partition FB1. The data signal and correlation to which the defect detection result outputted from said 1st partition Y string data output line XOY1 at this time is outputted from said 1st partition X string data output line XOX1 are made. Similarly, although omitted in drawing 2 , Y train selection signal line XSOY and the n-th partition Y string data output line XOYn other than said detection data output line OYn are connected to Y train selector YSn prepared in said n-th defect detection partition FBn (n is the integers from 2 to 90). The data signal and correlation by which the defect detection result outputted from said n-th partition Y string data output line XOYn at this time is outputted to said partition X string data output line XOXn are made. The same Y train select signal is inputted into Y train selector YS prepared in each of said defect detection partition FB of 90.
[0032] Each of said 1st partition X string data output line XOX1, the 1st partition Y string data output line XOY1, the 90th partition X string data output line XOX90, the 90th partition Y string data output line XOY90, the n-th partition X string data output line XOXn, and the n-th partition Y train output-data line XOYn is connected to the partition selector BS. In addition to this, the partition selection signal line BSK and X string data output line XOX, and Y string data output line XOY are connected to said partition selector BS. With the partition select signal inputted from said partition selection signal line BSK, said partition selector BS chooses a lot from **** of said n-th partition X string data output line XOXn and the n-th partition Y string data output line XOYn, and outputs it to said X string data output line XOX and Y string data output line XOY.
[0033] Drawing 3 is the block diagram showing the outline configuration of the defect detection partition of this example, and drawing 4 is the extention mimetic diagram of the defect detecting element of drawing 3 . Said 1st defect detection partition FB1 is mentioned as an example, and drawing 3 and drawing 4 show it. For the 1st data signal line, XSOX1, or XSOX6, in drawing 3 , X train selection signal line, XSOY1, or XSOY6 is [a decoding signal line, and IX101 and IX128 / DS1 thru/or DS5 / a detection data output line and S of Y train selection signal line, and OY1 and OY32] a slot, respectively. In drawing 4 , FG (x y) is a defect detection gate circuit.
[0034] The 1st defect detection partition FB1 of this example is constituted by the defect detecting element FA 1 by which said defect detection gate circuit was connected in the direction of X train, and the direction of Y train in the shape of a matrix, X train selector XS1, and Y train selector YS1 as shown in drawing 3 R> 3. It is the configuration same to the 90th defect detection partition FB90 from the remaining 2nd defect detection partition FB2 as said 1st defect detection partition FB1.
[0035] The defect detecting element FA 1 prepared in said 1st defect detection partition FB1 is divided in the direction of X train equivalent to the longitudinal direction in drawing 3 in the small region called 16 slots S in the direction of Y train which are 14 pieces and a lengthwise direction, and said two defect detection gate circuits FG are formed in each slot S. in order to distinguish hereafter each of the defect detection gate circuits FG established in said defect detecting element FA -- the location of the direction of X train, and the direction of Y train -- being shown (x y) -- it attaches and will be shown.
[0036] As said each defect detection gate circuit FG (x y) is shown in drawing 4 , it consists of test patterns connected between two 2 input NOR gates and them, and the test pattern which can detect poor opening and short [poor] to wiring which connects the outgoing end of the 1st step of 2 input NOR gate and the input edge of the 2nd step of 2 input NOR gate is formed. It connects with one [which is located in the latter-part side] input edge of the 1st step of 2 input NOR gate of a defect detection gate circuit, and the outgoing end of the 2nd step of each of said 2 input NOR gate from the defect detection gate circuit FG (1 1) located in a line in the direction of X train to the defect detection gate circuit FG (14 1) has the form where 28 2 input NOR gates were connected to the serial. The train which consists of 14 defect detection gate circuits connected to this serial hereafter is called a defect detection gate circuit train. Since there are 16 slots in the direction of Y train, the defect detection gate circuit train of 32 trains will be prepared in the defect detecting element FA 1 prepared in the 1st defect detection partition FB1 of this example.

[0037] As shown in drawing 4 , the 1st data signal lines [IX / IX and / 128] 101 are connected to the input edge of another side of 28 2 input NOR gates which make said defect detection gate circuit train sequentially from 2 input NOR gate of the last stage of each defect detection gate circuit train. However, both input edges are connected with the 1st data signal line IX 128 only for the 1st step of 2 input NOR gate of said defect detection gate circuit FG (14 y).
[0038] The outgoing end of the 2nd step of 2 input NOR gate of the defect detection gate circuit FG (1 y) of each defect detection gate circuit train of said 32 trains is connected with said Y train selector by the detection data output line OY1 thru/or OY32.
[0039] The 28 1st data signal lines [IX / IX and / 128] 101 which input a data signal into the defect detection gate circuit FG (x y) of said defect detecting element FA 1 are connected to the defect detection gate circuit formed in the defect detecting element of the following defect detection partition while connecting with X train selector XS1, as shown in drawing 3 .
[0040] With X train select signal which six X train selection signal lines XSOX1 thru/or XSOX6 are connected to said X train selector XS1, and is inputted into it from said X train selection signal line XSOX1 thru/or XSOX6 as shown in drawing 3 The inside of the data signal of said 1st data signal lines [IX / IX and / 128] 101, The data signal inputted into the defect detection gate circuit which is performing 14 defect detection gate circuits FG (1 y) of said defect detection gate circuit train thru/or poor opening in FG (14 y), or short [poor] is outputted to the 1st partition X string data output line XOX1.
[0041] Six Y train selection signal lines XSOY1 thru/or XSOY6 are connected to said Y train selector YS, and only one defect detection result in the defect detection result outputted from the detection data output line OY1 of each of said defect detection gate circuit train thru/or OY32 is outputted to the 1st partition Y string data output line XOY1 with Y train select signal inputted from said Y train selection signal line XSOY1 thru/or XSOY6. The data outputted from said 1st partition X string data output line XOX1 and the 1st partition Y string data output line XOY1 are inputted into the partition selector BS.
[0042] In said partition selector BS, like said 1st partition X string data output line XOX1 and the 1st partition Y string data output line XOY1 The n-th partition X string data output line XOXn from each of the remaining defect detection partition of 89 and the n-th partition Y string data output line XOYn are connected. The defect detection result based on the data signal inputted into the defect detection gate circuit FG (x y) used as the object for defect detection from each defect detection partition and the inputted data signal is inputted.
[0043] The group of the defect detection result based on the data signal which chose a lot from each defect detection partitions, and was inputted into the defect detection gate circuit used as the object for defect detection outputted from the selected defect detection partition in said partition selector BS by the partition select signal inputted from eight partition selection signal lines BSK1 thru/or BSK8, and the data signal which were inputted outputs to an X train output-data line XOX and a Y train output-data line XOY.
[0044] Drawing 5 is the representative circuit schematic showing the outline configuration of the defect detection gate circuit of this example. As for a transistor, and RE1, RCN1, RCP1, REFN1, RE2, RCN2, RCP2 and REFN2, in drawing 5 , a resistance element, and C1 and C2 are [Q0, Q1, Q2 Q3, QAD1, QEN1, Q4, Q5, Q6, Q7, QAD2, and QEN2] capacitative elements.
[0045] The 1st step of NOR gate which consists of transistors Q0, Q1, Q2, Q3, QAD1, and QEN1, resistance elements RE1, RCN1, RCP1, and REFN1, and capacitative elements C1 as the defect detection gate circuit of this example is shown in drawing 5 , The two NOR gates of the 2nd step of NOR gate which consists of transistors Q4, Q5, Q6, Q7, QAD2, and QEN2, resistance elements RE2, RCN2, RCP2, and REFN2, and capacitative elements C2, It is constituted by the test pattern which can detect poor opening and short [poor] which were formed between the emitter electrode of the transistor QEN1 which is the outgoing end of said 1st NOR gate, and the base electrode of the transistor Q4 which is one input edge of said 2nd NOR gate.
[0046] Drawing 6 thru/or drawing 10 are the ** type top views and sectional views showing the outline configuration of the defect detection gate circuit of this example, drawing 6 thru/or drawing 9 are the **

type top views having divided and shown the configuration of the test pattern formed in said defect detection gate circuit for every wiring layer, and drawing 10 is type section drawing in the A-A' line in the condition of having carried out the laminating of each wiring layer shown in drawing 6 thru/or drawing 9 .

[0047] In drawing 6 thru/or drawing 10 IX01 and IX02, respectively The 1st data signal line, Metal wiring for defect detection and SCL2 FCL Wiring for poor short detection of the 2nd wiring layer, Wiring for poor short detection of the 3rd wiring layer and SCL4 SCL3 Wiring for poor short detection of the 4th wiring layer, Wiring for poor short detection of the 5th wiring layer, TH1, TH1A, and TH1B SCL5 The 1st through hole, TH2 the 3rd through hole and TH4 for the 2nd through hole and TH3 The 4th through hole, PVTT, and P3, P4 and P5 -- for the 1st interlayer insulation film and 2, as for the 3rd interlayer insulation film and 4, the 2nd interlayer insulation film and 3 are [the pad for failure analyses, and BS / a semi-conductor substrate and 1 / the 4th interlayer insulation film and 5] surface protective coats.

[0048] As said test pattern is shown in drawing 6 thru/or drawing 10 The 2nd through hole TH2 formed in the 2nd interlayer insulation film 2 in two or more metal wiring FCL for poor detection formed in each of the 2nd wiring layer to the 5th wiring layer on a semi-conductor substrate, It has connected through the 3rd through hole TH3 formed in the 3rd interlayer insulation film 3, and the 4th through hole TH4 formed in the 4th interlayer insulation film 4. the defect detection connected through said each through hole -- public funds -- the end of the group wiring FCL is connected with the emitter electrode of the transistor QEN1 shown in said drawing 5 through 1st through hole TH1A shown in drawing 6 and drawing 10 . The other end of said metal wiring FCL for defect detection is connected with the base electrode of the transistor Q4 shown in said drawing 5 through 1st through hole TH1B shown in drawing 6 .

[0049] As said metal wiring FCL for poor detection formed in each wiring layer is shown in drawing 6 thru/or drawing 10 , the wiring SCL for poor short detection is formed so that each metal wiring FCL for poor detection may be adjoined. Said wiring SCL for poor short detection is divided and formed in each of the wiring SCL2 for poor short detection of the 2nd wiring layer, the wiring SCL3 for poor short detection of the 3rd wiring layer, the wiring SCL4 for poor short detection of the 4th wiring layer, and the wiring SCL5 for poor short detection of the 5th wiring layer, and poor short detection can be carried out now for every wiring layer.

[0050] Moreover, the pad PVTT for failure analyses pulled out from each wiring layer as shown in drawing 9 , and P3, P4 and P5 are prepared in the 5th wiring layer. Said each pad for failure analyses is pulled out from each wiring layer, and can specify the wiring layer which has a poor open circuit by carrying out flow inspection between each failure-analysis pad.

[0051] Moreover, the 1st data signal lines IX01 and IX02 as shown in drawing 6 other than said metal wiring FCL for poor detection and the wiring SCL for poor short detection, power-source wiring, etc. are formed in said each wiring layer (not shown).

[0052] Drawing 11 is a mimetic diagram for explaining the defect detection approach by the gate matrix TEG of this example, and is drawing for explaining the defect detection approach in one defect detection gate circuit.

[0053] drawing 11 -- setting -- FG -- a defect detection gate circuit, and IXA and IXB -- a data signal line and FCL -- defect detection -- public funds -- for wiring for poor short detection of the 3rd wiring layer, and SCL4, wiring for poor short detection of the 4th wiring layer and SCL5 are [group wiring and SCL2 / wiring for poor short circuit detection of the 2nd wiring layer, and SCL3 / a low-power output signal and H of wiring for poor short detection of the 5th wiring layer and L] high power signals. In this example, said low-power output signal L is made into 0 volt (V), and said high power signal H is made into 5 volts (V).

[0054] In detecting poor opening using said defect detection gate circuit FG, the data signal inputted into the 1st step and the 2nd step of NOR gate of said defect detection gate circuit FG is made into the low-power output signal L from the data signal lines IXA and IXB, and it makes it the signal inputted into said the 1st step of NOR gate also turn into the low-power output signal L from the defect detection gate

circuit of the preceding paragraph. Moreover, the low-power output signal L is inputted into the wiring SCL2 for poor short detection of each of said wiring layer thru/or SCL5. this time -- the 1st step of defect detection from the NOR gate -- public funds -- since the output to the group wiring FCL is the high power signal H -- said defect detection -- public funds -- if there is no open circuit in the group wiring FCL, it will become the low-power output signal L and the high power signal H to be inputted into the 2nd step of NOR gate. Therefore, the 2nd step of output of the NOR gate serves as the low-power output signal L. It turns out that an output serves as the high power signal H since the low-power output signal L will be inputted into the 2nd step of NOR gate if said metal wiring FCL for poor detection is disconnected, and the defect detection gate circuit FG has poor opening.

[0055] In detecting short [poor] using said defect detection gate circuit FG, the data signal into which the data signal inputted into the 2nd step of NOR gate of said defect detection gate circuit FG from said data signal line IXA is inputted in the 1st step of NOR gate from the low-power output signal L and said data signal line IXB is made into the high power signal H, and it makes it the signal inputted into said the 1st step of NOR gate from the defect detection gate circuit of the preceding paragraph, turn into the low-power output signal L on the other hand. And the high power signal H is inputted into any one [SCL2] of the SCL(s)5, for example, wiring for poor short detection of the 2nd wiring layer, from the wiring SCL2 for poor short detection prepared in each from the 2nd wiring layer to the 5th wiring layer. this time -- said the 1st step of said defect detection from the NOR gate -- public funds -- since the output to the group wiring FCL is the low-power output signal L -- said defect detection -- public funds -- if the group wiring FCL and the wiring SCL2 for poor short detection of the 2nd wiring layer do not touch, it becomes the low-power output signal L to be inputted into said the 2nd step of NOR gate. Therefore, the 2nd step of output of the NOR gate serves as the high power signal H. If said metal wiring FCL for poor detection and wiring SCL2 for poor short detection of said 2nd wiring layer touch The high power signal H from said wiring SCL for poor short detection flows to said metal wiring FCL for defect detection. The low-power output signal L and the high power signal H will be inputted into said the 2nd step of NOR gate, said the 2nd step of output of the NOR gate becomes the low-power output signal L, and it turns out that the defect detection gate circuit FG has short [poor] in the 2nd wiring layer. By carrying out similarly, even if it attaches by the 5th wiring layer from the 3rd wiring layer, it can specify which wiring layer of the defect detection gate circuit FG has short [poor].

[0056] Drawing 12 and drawing 13 are drawings for explaining the detection approach of poor opening by the gate matrix TEG of this example, and short [poor]. As for IX01 thru/or IX28, in drawing 12 and drawing 1313 , a data signal line and OY1 are detection data output lines. Said data signal lines [IX / IX and / 28] 01 are equivalent to the 1st data signal lines [IX / IX and / 128] 101 shown in said drawing 3 .

[0057] First, Y train selector prepared in each defect detection partition inputs Y train select signal so that the defect detection result from the defect detection gate circuit train OY1, i.e., said detection data output line, of eye one train may be outputted.

[0058] Next, as shown in drawing 12 (a), the low-power output signal L is outputted from the detection data output line OY1 of a defect detection gate circuit train in this condition of inputting the high power signal H into said all data signal lines [IX / IX and / 28] 01, and inputting the low-power output signal L into the wiring SCL2 for poor short detection thru/or SCL5. Although omitted in drawing 12 (a), the low-power output signal L is similarly outputted from each detection data output line of the defect detection gate circuit train of the 31 remaining trains of each defect detecting element.

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing showing the outline configuration of the semiconductor integrated circuit equipment which carried process evaluation TEG of the example by this invention.
[Drawing 2] It is the ** type block diagram showing the outline configuration of the gate matrix TEG of this example.
[Drawing 3] It is the ** type block diagram showing the outline configuration of the defect detection partition of this example.
[Drawing 4] It is the mimetic diagram showing the outline configuration of the defect detecting element of this example.
[Drawing 5] It is the representative circuit schematic showing the outline configuration of the defect detection gate circuit of this example.
[Drawing 6] It is the ** type top view showing the outline configuration of the defect detection gate circuit of this example.
[Drawing 7] It is the ** type top view showing the outline configuration of the defect detection gate circuit of this example.
[Drawing 8] It is the ** type top view showing the outline configuration of the defect detection gate circuit of this example.
[Drawing 9] It is the ** type top view showing the outline configuration of the defect detection gate circuit of this example.
[Drawing 10] It is type section drawing showing the outline configuration of the defect detection gate circuit of this example.
[Drawing 11] It is a mimetic diagram for explaining the defect detection approach using the defect detection gate circuit of this example.
[Drawing 12] It is drawing for explaining the defect detection approach by the gate matrix TEG of this example.
[Drawing 13] It is drawing for explaining the defect detection approach by the gate matrix TEG of this example.
[Description of Notations]
CH [-- Defect detection partition field,] -- A semiconductor chip, B -- A partition, FB -- A defect detection partition, FBA D -- A decoder circuit, BS -- A partition selector, RT--RAM assessment TEG FA -- A defect detecting element, a XS--X train selector, a YS--Y train selector, IX -- Data signal line, A XSOY--X train selection signal line, a XSOY--Y train selection signal line, XOX1-XOX90 -- Partition X string data output line, XOY1-XOY90 -- A partition Y string data output line, OY -- Detection data output line, A XOX--X string data output line, a XOY--Y string data output line, DS -- Decoding signal line, BSK -- A partition selection signal line, S -- A slot, FG (x y) -- Defect detection gate circuit, Q0-Q7, QAD1, QEN1, QAD2, QEN2 -- Transistor, RE1, RCN1, RCP1, REFN1, RE2, RCN2, RCP2, REFN2 -- Resistance element, C1, C2 -- A capacitative element, FCL -- Metal wiring for poor detection, SCL2-SCL5 -- Wiring for poor short detection, TH1, TH1A, TH1B [-- The 4th through

hole, PVTT, P3, P4, P5 / -- The pad for failure analyses, BS / -- A semi-conductor substrate, 1 2, 3, 4 / -- An interlayer insulation film 5 / -- Surface protective coat] -- The 1st through hole, TH2 -- The 2nd through hole, TH3 -- The 3rd through hole, TH4

[Translation done.]

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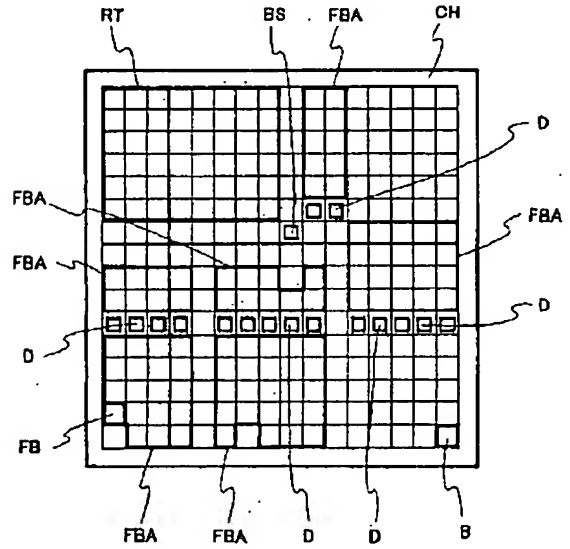
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]

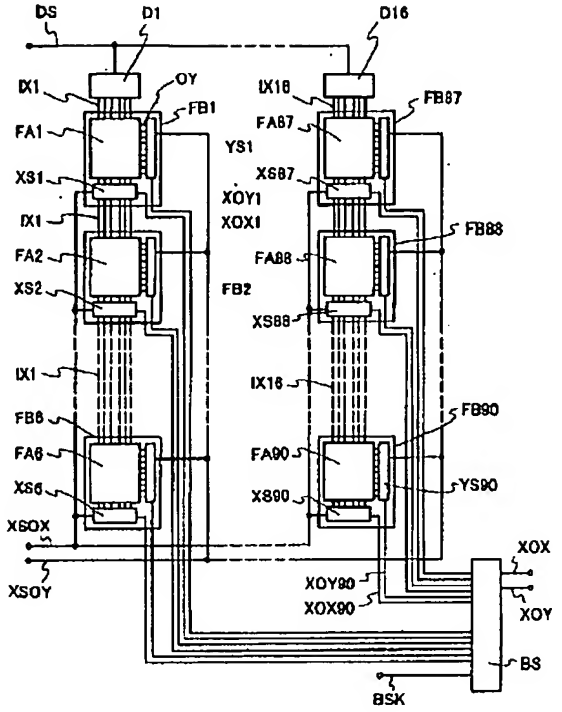
図1



CH:半導体チップ
B:区画
FB:不良検出区画
FBA:不良検出区画領域
D:デコーダ回路
BS:区画セレクタ回路
RT:RAM評価TEG

[Drawing 2]

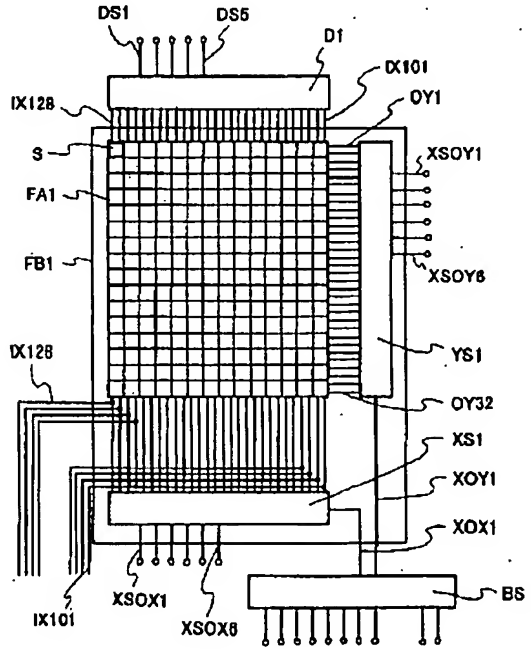
図2



FA1～FA90:不良検出部
XS1～XS90:X列セレクタ
YS1～YS90:Y列セレクタ
D1, D16:デコード信号線
IX1,IX16:データ信号線
OY:検出データ出力線
XSOX:X列セレクト信号線
XSOY:Y列セレクト信号線
BSK:区間セレクト信号線
XOX1,XOX90:区間X列データ出力線
XOY1,XOY90:区間Y列データ出力線
XOX:X列データ出力線
XOY:Y列データ出力線

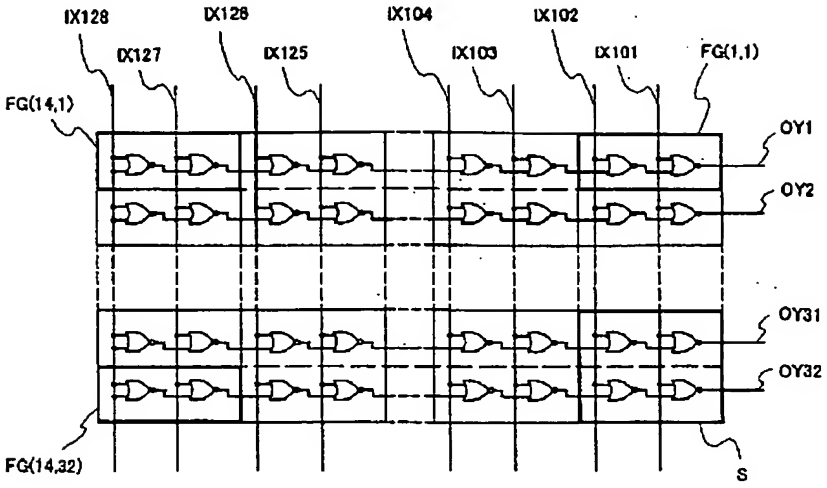
[Drawing 3]

図3



[Drawing 4]

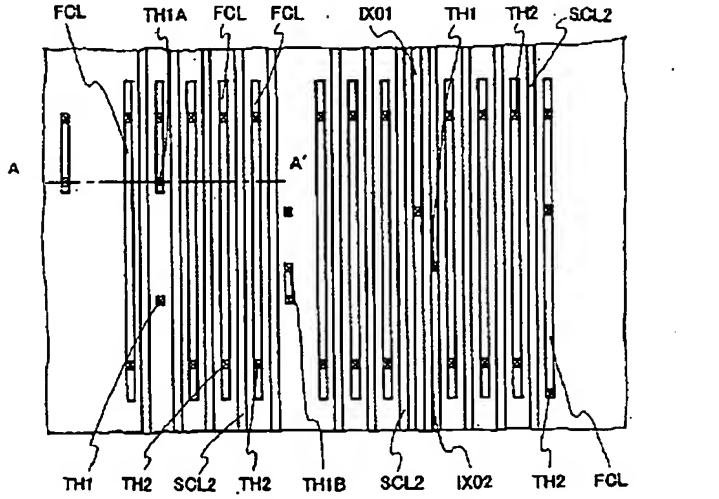
図4



FG(x,y):不良検出ゲート回路

[Drawing 6]

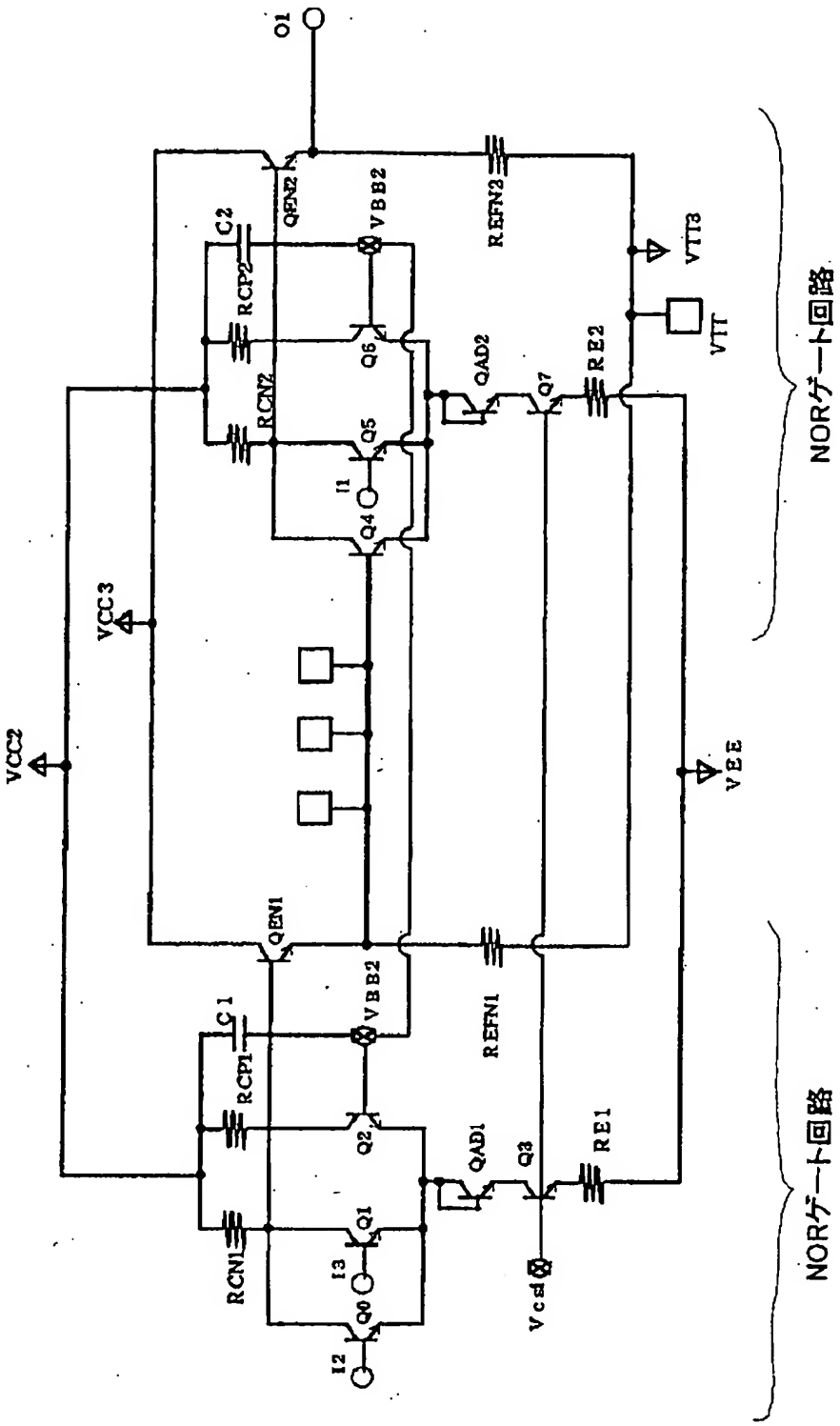
図6



FCL:不良検出用金属配線
SCL2:第2配線層のショート不良検出用配線
TH1,TH1A,TH1B:第1スルーホール
TH2:第2スルーホール

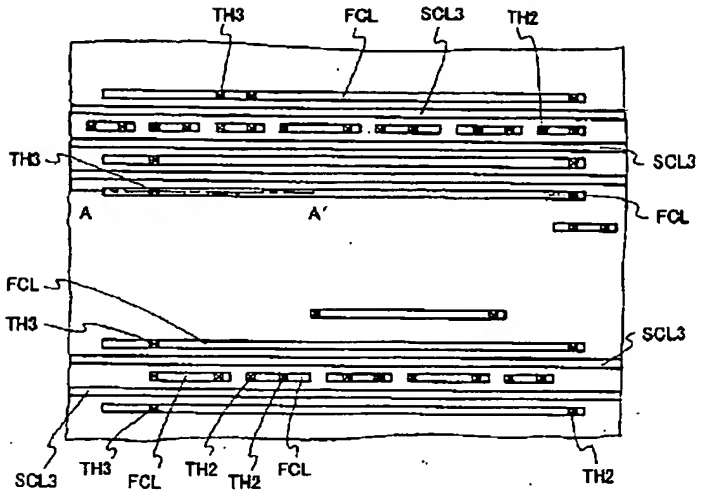
[Drawing 5]

図5


O1
QEN2
VBB2
C2
RCP2
RCN2
Q6
Q5
I1
Q4
QAD2
Q7
RE2
REFN2
VTT3
VTT
NORゲート回路
VCC3
VCC2
VEE
QEN1
VBB2
C1
RCP1
RCN1
Q2
Q1
I3
Q0
I2
QAD1
Q3
RE1
REFN1
Vcs
NORゲート回路

[Drawing 7]

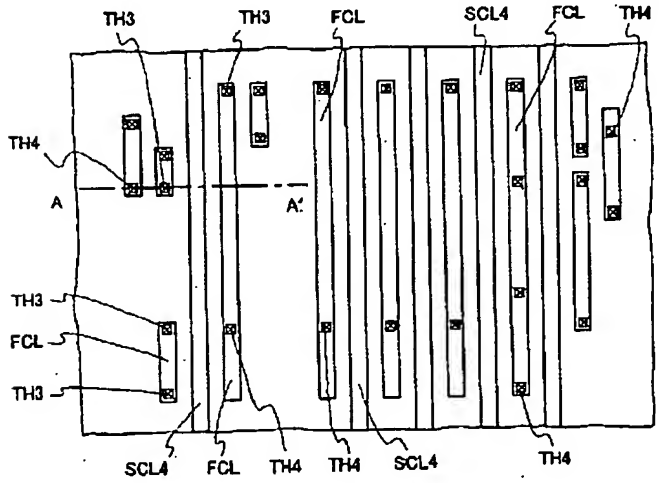
図7



SCL3: 第3配線層のショート不良検出用配線
TH3: 第3スルーホール

[Drawing 8]

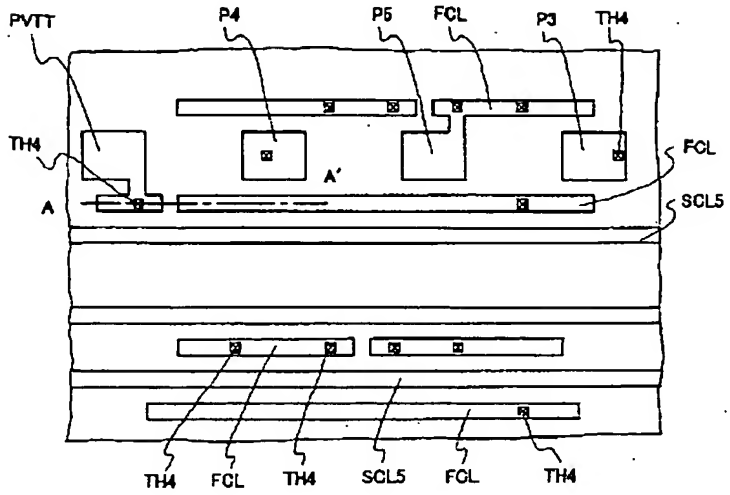
図8



SCL4: 第4配線層のショート不良検出用配線
TH4: 第4スルーホール

[Drawing 9]

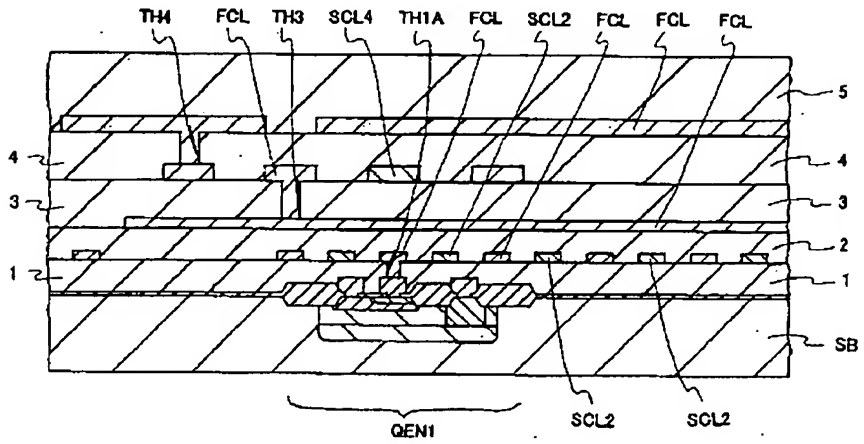
図9



SCL5:第5配線層のショート不良検出用配線
PVTT,P3,P4,P5:不良解析用パッド

[Drawing 10]

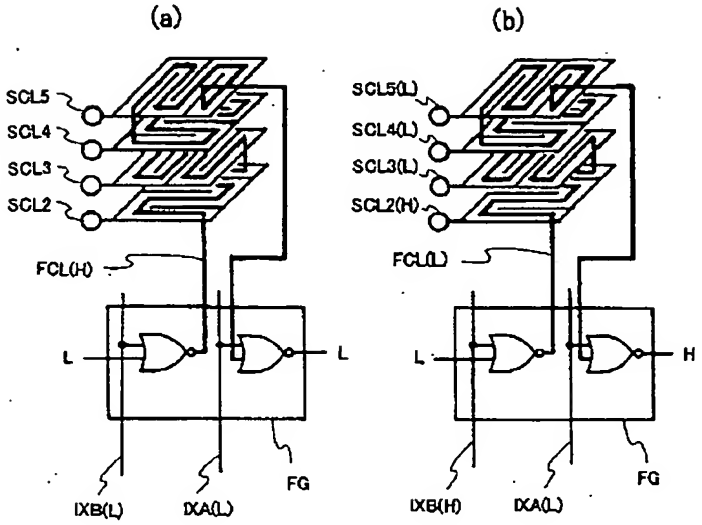
図10



SB:半導体基板
1,2,3,4:層間絶縁膜
5:表面保護膜

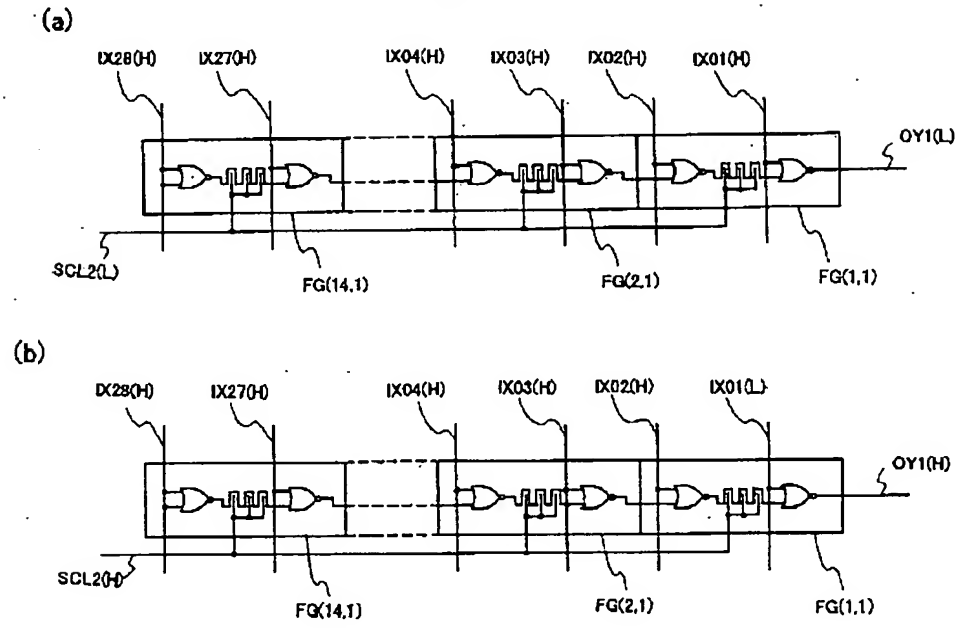
[Drawing 11]

図11



[Drawing 12]

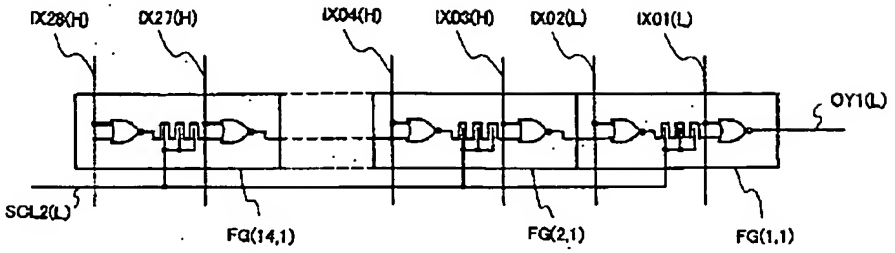
図12



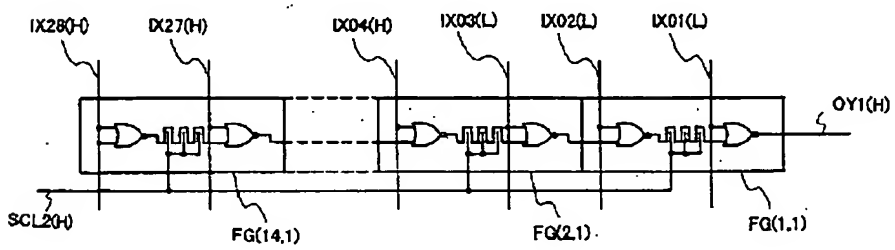
[Drawing 13]

図13

(c)



(d)



[Translation done.]